32.6 A Reversible Poly-Phase Distributed VCO

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Voltage Controlled Oscillators (VCOs) based on *LC* tanks have emerged as the primary design choice for applications in wireless, wireline, and optical communications that operate at high frequency and require low phase noise. Lumped *LC* VCOs generate up to four clock phases [1]. VCOs that generate eight or more phases enable quarter rate and/or over-sampled receiver architectures, relaxing the bandwidth requirement on the front end. Distributed VCOs are suitable for generating eight or more phases. A distributed VCO can be constructed from a distributed amplifier with its output fed back to its input [2], but both the input and output transmission lines (T-lines) must be terminated, increasing the phase noise and limiting the voltage swing. A closed-loop distributed VCO [3] overcomes these problems since the T-line does not require termination. However, closed-loop distributed VCOs are circularly symmetric, leading to uncertainty pertaining to the clock phase direction, i.e., clockwise or counterclockwise. In this paper, we present a 24-phase distributed VCO with a built-in mechanism to control the clock direction. The proposed circuit topology can be used to deliver an arbitrary even number of clock phases.

The VCO architecture (Fig. 32.6.1) is based on a folded co-planar T-line divided into 24 equal-length segments such that consecutive clock phases are separated by 15° and opposite clock phases are adjacent. Consequently, the 24 phases are delivered as 12 differential pairs (clk_i and $\overline{clk_i}$, i=0,...,11). Twelve negative-g_m circuits connecting each clk_i and $\overline{clk_i}$ pair start and sustain the oscillation. Buffers drive $clko_i$ and $\overline{clko_i}$ from clk_i and $\overline{clk_i}$. The VCO frequency is adjusted by a voltage control signal, V_{ctl}, that spans the entire VCO.

A distributed VCO is useful only if its direction can be controlled. After power up, whether clk_i leads or trails clk_{i-1} depends on the order that the stages are powered up, which depends on the location of the supply pads, the supply distribution network, and the physical arrangement of the LC lines. Since it is difficult to account for these considerations at design time, a circuit to control phase sequence is needed. Figure 32.6.2 shows the circuit used (with the output buffers omitted for clarity). In each stage, two nFETs are added that conditionally pull down clk_i and $\overline{clk_i}$. When on, these nFETs add positive resistance that cancels out the negative-g_m circuits. Their gates are controlled by signal rst_0/rst_{11} starting with clk_0 and ending with $\overline{clk}_{11}$ or the other way around, following the VCO loop. Pulling up the control signal stops the VCO from oscillating and resets the clock phases to a dc voltage determined by the strength of the FETs in the negative-g_m circuit and the positive-resistance nFETs. After all phases are reset, the control signal is pulled down either from the rst_0 side (clk_0 leads) or from the rst_{11} side ($\overline{clk_{11}}$ leads), releasing the clock phases in a pre-determined order. Ideally, delay through each LRC block should match the corresponding VCO T-line segment delay. Replicating the VCO T-line for the control signal would incur an unnecessary area penalty, since the T-lines are very wide to maximize Q. Circuit simulation indicated that the circuit operates successfully for a wide range of control signal wire delays, and a much more compact control-line layout was used with delay similar to the T-line delay. This circuit has some advantages over an alternative circuit that has been used in a quadrature lumped LC VCO [4] and could be adapted for a distributed VCO. First, in our circuit, the added nFETs are on only during reset and do not contribute to the VCO phase noise. Second, they are relatively small devices contributing little to the VCO internal capacitance.

Figure 32.6.3 shows the circuitry required for each VCO stage i, except the T-lines. Cross-coupled FETs MN_0, MP_0, MN_1, and MP_1 form the negative-g_m circuit. Common-source buffers drive the clock loads $clko_i$ (MN_2/MP_2) and $\overline{clko_i}$ (MN_3/MP_3). Each stage contains two sets of MOS varactors (MV_0 and MV_1) that adjust the VCO frequency based on V_{ctl}. MN_4 and $\overline{MN_5}$ are the positive-resistance nFETs. Signals $rstd_i$ and $\overline{rstd_i}$ are the delayed control signals.

The VCO (Fig. 32.6.4) was implemented in a 10-metal, triple-well, 90-nm, 1.2V CMOS ASIC process. A 60Ω metal-10 T-line with manually inserted dummy metal enclosed in a U-shaped ground return down to metal-2 allowed circuits to be placed directly underneath. Compared to an artificial LC T-line, using U-shielded real T-lines greatly simplifies floor-planning and eliminates the need to model coupling between inductors. Each VCO stage is 208μm long, with adjustments made to the corners. The VCO size is 1.4mm by 0.25mm. Each VCO output ($clko_i$ *and* $\overline{clko_i}$) drives an open-drain nFET, with drains driven by $clko_2$, $clko_4$, $clko_7$, and $\overline{clko_9}$ connected to I/O pads for probing using external bias-tees. Our RF prober allows us to simultaneously observe two phases. The VCO operation was controlled externally by setting its inputs $\overline{rst_0}$, osc_0, $\overline{rst_{11}}$, and osc_{11} (Fig. 32.6.2) through a scan register.

The measured VCO frequency (Fig. 32.6.5) ranges from 10.41 to 11.37GHz for a 1.2V control voltage sweep. With Vctl = 0V, we measured phase noise of -96.65dBc/Hz at a 1MHz offset (Fig. 32.6.6). An earlier version of the same VCO architecture exhibited a lower phase noise (-101.58dBc/Hz at 1MHz) with a smaller frequency range (0.35GHz). To boost the frequency range, more varactors were added and the T-lines were shortened to compensate for the increased capacitance, which deteriorated the phase noise. Power dissipation was 70mW including the bias circuit.

Phase reversal was demonstrated (Fig. 32.6.7) by triggering an oscilloscope with a divided-by-8 $\overline{clko_9}$ and displaying $clko_4$ for both clockwise and counterclockwise oscillation. With this set-up we can measure the phase shift for $clko_4$ when $clko_0$ is the lead phase (counterclockwise) versus when $\overline{clko_{11}}$ is the lead phase (clockwise). Neither cables nor probes were moved during the measurements to avoid introducing an error due to phase shift in the path to the oscilloscope. As shown in Fig. 32.6.1, when $clko_0$ is the lead phase, $clko_4$ leads $\overline{clko_9}$ by 225°, otherwise $\overline{clko_9}$ leads $clko_4$ by 225°. By using $\overline{clko_9}$ to derive the trigger point, there is a theoretical 510° phase difference between $clko_4$ and its reverse phase, or 150° after subtracting the 360° of a full cycle. The measured phase difference is 158° before correction, or 151° after correcting for the misaligned trigger displayed by the oscilloscope after the traces were superimposed. Similar results were obtained for $clko_2$.

Acknowledgments:
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References:
[1] A. Rofougaran, et al., "A 900 MHz CMOS LC-Oscillator with Quadrature Outputs," *IEEE ISSCC Dig. Tech. Papers,* pp. 392-393, Feb., 1996.
[2] W. Wu et al., "Silicon-Based Distributed Voltage-Controlled Oscillators," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 493-502, Mar., 2001.
[3] J. Lee et al., "A 40-Gb/s Clock and Data Recovery Circuit in 0.18-μm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2181-2190, Dec., 2003.
[4] S. Gierkink et al., "A Low-Phase-Noise 5GHz Quadrature CMOS VCO using Common-Mode Inductive Coupling," *ESSCIRC*, pp. 539-542, Sept., 2002.

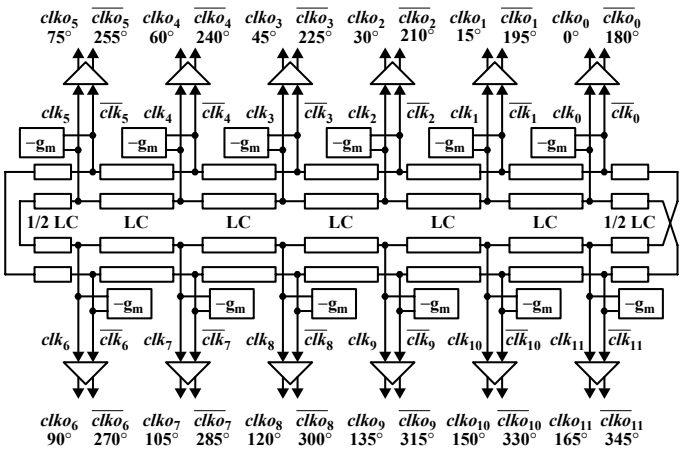

Figure 32.6.1: Poly-phase VCO architecture.

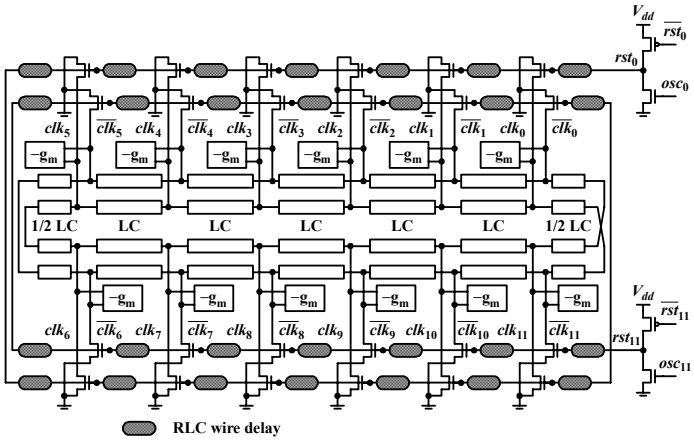

Figure 32.6.2: Controlling VCO oscillation and phase sequence.

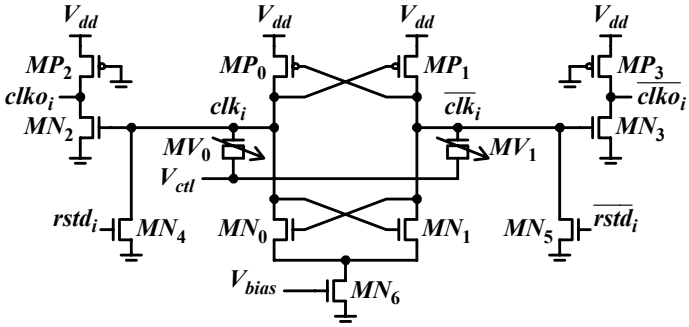

Figure 32.6.3: Negative-g_m circuit including common-source clock buffers, varactors, and positive-resistance nFETs.

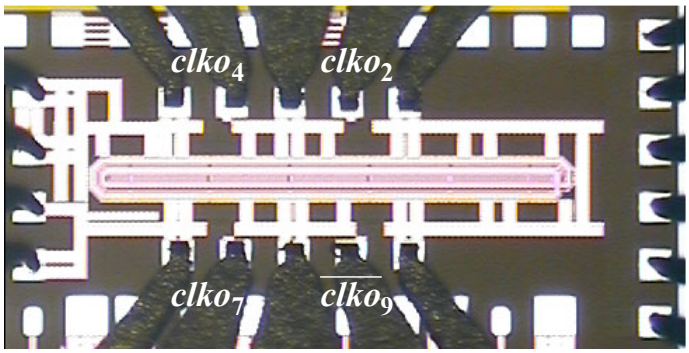

Figure 32.6.4: VCO micrograph.

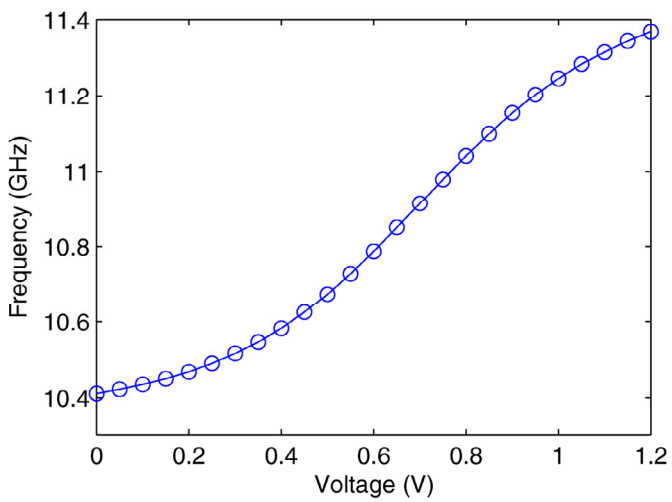

Figure 32.6.5: Measured frequency range versus voltage.

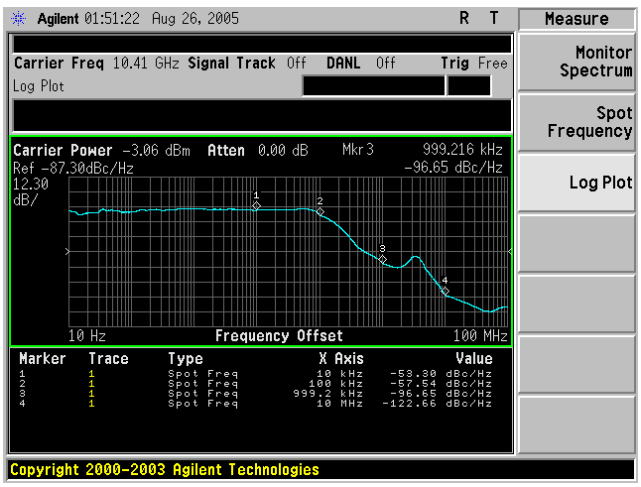

Figure 32.6.6: Measured VCO phase noise.

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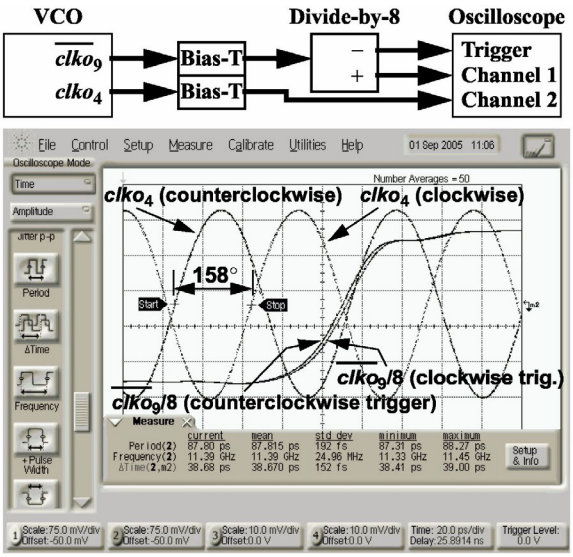

Figure 32.6.7: Demonstration of phase sequence reversal.

